

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**Docket No. 13464US04**

In The Application Of:

ESIN TERZIOGLU et al.

Serial No.: To be assigned

Filed: herewith

Examiner: To be assigned

Group Art Unit: 2824

For: MEMORY ARCHITECTURE WITH  
SINGLE PORT CELL AND DUAL  
PORT (READ AND WRITE)  
FUNCTIONALITY

**CERTIFICATE OF MAILING**

Date of Deposit: July 2, 2003

I hereby certify that the attached  
paper or fee is being deposited with the  
United States Postal Service as Express  
Mail, No. EV 164032397 US on the date  
indicated above and addressed to the  
Commissioner for Patents, PO Box  
1450, Alexandria, VA 22313-1450.

By: Ronald E. Larson  
Ronald E. Larson  
Reg. No. 24,478

**PRELIMINARY AMENDMENT**

Commissioner for Patents  
PO Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Kindly amend the above-identified application as follows:

**In the Specification:**

On page 1, immediately after the heading "CROSS-REFERENCE TO RELATED APPLICATIONS (S)" kindly insert the following new paragraph:

This is a continuation of U.S. Application No. 10/173,709 filed June 18, 2002 filed under docket no. 13464US03.

Please replace the second full paragraph on page 2, lines 6-18, with the following paragraph:

Memory Module with Hierarchical Functionality, Attorney Docket No. 13441US02, Serial No. 09/775,477; High Precision Delay Measurement Circuit, Attorney Docket No. 13447US02, Serial No. 09/776,262; Single-Ended Sense Amplifier With Sample-And-Hold Reference, Attorney Docket No. 13435US02, Serial No.